In re Patent Application of:
ZENG
Serial No. **09/844,347**
Filing Date: **April 27, 2001**
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Please replace the paragraph beginning at page 9, line 28, with the following rewritten paragraph:

A2

-- A dielectric layer 76 is deposited on the surface of the gate dielectric layer 24 and on the surface of the gate 12. The dielectric layer 76 is for isolating the gate 12. The surface dielectric layer 76 is removed, and the upper surface of the body region 16 and the upper surface of the dielectric layer 20 within the trench 14 are planarized, as illustrated in FIG. 8. --

Please replace the paragraph beginning at page 10, line 14, with the following rewritten paragraph:

A3

-- Surface portions laterally adjacent the dielectric layer are removed so that a portion of the dielectric layer 20 extends outwardly therefrom, as illustrated in FIG. 9. A thickness of the surface portions that is removed is within a range of about 0.1 to 1 micron. As will be explained in greater detail below, the outwardly extending dielectric layer 20 advantageously allows self-aligned spacers to be formed. --

Please insert the following paragraph on page 14, between lines 18 and 19:

A4

-- Referring now to FIG. 16, the top plan view of the trench-gated power MOSFET **70** illustrates that the source/body contact regions are laterally spaced apart from